CBCS SCHEME

USN | | | | | | | | | | |

15NT54

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is Multiplexer? Explain the working of 2:1 multiplexer with truth table and logic diagram. **(08 Marks)**

b. What is Full adder? Design a binary Full adder with a truth table. Write the Boolean expression for output. **(08 Marks)**

OR

2 a. Write a verilog code for AND gate using data flow, behavioural flow and structural flow methods. **(06 Marks)**

b. With the help of diagram and truth table explain full subtractor. Write the output Boolean expressions. **(06 Marks)**

c. Differentiate combinational and sequential circuits. **(04 Marks)**

Module-2

3 a. Write note on purity bit generator. **(08 Marks)**

b. Describe the operation of ripple carry adder with block diagram and logic diagram. **(08 Marks)**

OR

4 a. Write a note on 4-bit carry look ahead adder. **(06 Marks)**

b. Explain the operation of 3-bit Rotators using multiplexer. **(05 Marks)**

c. Write note on Barel shifter using 2:1 multiplexer. **(05 Marks)**

Module-3

5 a. Explain the working of D-latch using NOR gate with truth table and logic diagram. **(08 Marks)**

b. Define shift register. Discuss about Parallel In Parallel Out (PIPO) shift register with diagram. **(08 Marks)**

OR

6 a. Explain the working of Asynchronous counter. **(08 Marks)**

b. Explain T-latch with circuit diagram and Truth table. **(08 Marks)**

Module-4

7 a. Explain realization of CMOS OR gate and AND gate. **(08 Marks)**

b. Explain the power dissipation equation for CMOS. **(06 Marks)**

c. Explain noise margin in CMOS. **(02 Marks)**

OR

8 a. Explain realization of CMOS XOR and XNOR gate. **(08 Marks)**

b. Discuss CMOS transmission gates and multiplexer. **(08 Marks)**

Module-5

9 a. Write a verilog HDL code for SR and D flip flop. **(10 Marks)**

b. How to write a verilog code for up/down counters? **(06 Marks)**

OR

10 a. Write a note on Programmable Logic Array (PLA) and Field Programmable Gate Array (FPGA). **(12 Marks)**

b. Explain the method of writing a verilog code for latch. **(04 Marks)**

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